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EXAMINER	
HUISMAN, DAVID J	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,904	VANNERSON ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) *10-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 18-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 18-29 have been examined. Claims 10-17 have been withdrawn from consideration for reasons described below.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9 and 18-29, drawn to apparatus and methods for attaching a breakpoint bit to each instruction and/or attaching breakpoint register bits to a control status register, classified in class 712, subclass 227.

II. Claims 10-17, drawn to an array processor having a decoder to decode a breakpoint bit attached to each instruction and to decode breakpoint register bits attached to a control status register, classified in class 712, subclass 10.

The inventions are distinct, each from the other because of the following reasons:

3. Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct if they do not overlap in scope and are not obvious variants, and if it is shown that at least one subcombination is separately usable. In the instant case, subcombination I has separate utility such as attaching breakpoint bits to instructions in any type of processor (not just an array processor having multiple processor elements. Also, the attachment of breakpoint bits is not concerned with how these bits are decoded. See MPEP § 806.05(d).

The examiner has required restriction between subcombinations usable together. Where applicant elects a subcombination and claims thereto are subsequently found allowable, any

claim(s) depending from or otherwise requiring all the limitations of the allowable subcombination will be examined for patentability in accordance with 37 CFR 1.104. See MPEP § 821.04(a). Applicant is advised that if any claim presented in a continuation or divisional application is anticipated by, or includes all the limitations of, a claim that is allowable in the present application, such claim may be subject to provisional statutory and/or nonstatutory double patenting rejections over the claims of the instant application.

4. Because these inventions are independent or distinct for the reasons given above and there would be a serious burden on the examiner if restriction is not required because the inventions require a different field of search (see MPEP § 808.02), restriction for examination purposes as indicated is proper.

5. During a telephone conversation with Mr. Steven Laut, Reg. No. 47,736, on June 14, 2007, a provisional election was made with traverse to prosecute the invention of group I, claims 1-9 and 18-29. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-17 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. The abstract of the disclosure is objected to because not only is it replete with sentence fragments and grammatical errors, but it does not sufficiently describe the disclosure and, therefore, does not assist readers in deciding whether there is a need for consulting the full patent

text for details. The examiner requests that a new, grammatically correct, and detailed abstract be submitted. Correction is required. See MPEP § 608.01(b).

8. The disclosure is objected to because of the following informalities:

- On page 1, the headings above paragraphs [0001] and [0002] should be made to look similar to the remaining headings in the disclosure.
- On page 5, paragraph [0024], line 2, insert --to-- after "coupled".
- On page 7, paragraph [0032], reference number 781 is associated with the debug executive unit. However, component 781 is a multiplexer in Fig.7A.
- On page 10, paragraph [0047], it is not clear if the phrase "biological electrical, mechanical systems" is a typographical error or not. The examiner is unsure what applicant is disclosing with this phrase.

Appropriate correction is required.

Drawings

9. The drawings are objected to because of the following minor informalities:

- In Fig.4, please label each of the components. For instance, component 410 should be labeled as "Memory".
- In Fig.8A, replace reference number 810 with --800--.
- In Fig.8A, step 870, replace "STORE" with --STOP--.
- In Fig.8A, steps 840, 850, 860, and 880, the examiner feels is would be more clear to delete the word "IS" from each step and replace the phrase "DETERMINE IF" from each step with --IS THE--.

- In Fig.8B, in both portions, it is not clear what is meant by loading LDTI/LDFI into debug instruction. How is an instruction loaded into an instruction?

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

10. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

- In Fig.7, reference numbers 700, 710, and 780 do not appear.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of

an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

11. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- In Fig.8, reference number 865 does not appear in the specification.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

12. Claim 5 is objected to because of the following informalities: Please insert --wherein-- before "said" in line 1. Appropriate correction is required.

13. Claim 6 is objected to because of the following informalities: Please insert --wherein-- before "said" in line 1. Appropriate correction is required.

Claim Rejections - 35 USC § 101

14. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

15. Claims 18-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. On page 10, paragraph [0047], of the specification, applicant has provided evidence that applicant intends the machine-readable medium of claims 18-23 to include transmission waves and signals. Consequently, the claims are drawn to a form of energy. Energy is not a series of steps of acts and thus is not a process. Energy is not a physical article or object and as such is not a machine or manufacture. And finally, energy is not combination of substances and therefore not a composition of matter. Since energy is not one of the four categories of invention, claims 18-23 are non-statutory.

Claim Rejections - 35 USC § 112

16. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

17. Claims 4, 18, and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, each of the aforementioned claims is unclear because the examiner does not know what is meant by

attaching at least three fields to a control status register. The examiner asserts that unless the processor is reconfigurable, which applicant's specification gives no indication of, a register is a fixed hardware component. Additional hardware cannot be dynamically attached to pre-existing hardware. Does applicant instead mean that at least three bits of a register are set? Fig.6 shows that bits are added onto a register but the examiner is not sure how this is done without undue experimentation.

18. Claims 5-6, 19-23, and 25-29 are rejected under 35 U.S.C 112, 1st paragraph, for being non-enabling, because they are dependent, either directly or indirectly, on a non-enabling claim.

19. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

20. Claims 2-3, 7-8, 19, and 23-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. Claim 2 recites the limitation "said breakpoint bit" in line 1. There is insufficient antecedent basis for this limitation in the claim because claim 1 claims "at least one breakpoint bit". Therefore, when multiple breakpoint bits exist, it is not clear which of the bits "said breakpoint bit" refers to.

22. Claims 7-8 recite the limitation "said at least one processor" in line 1. There is insufficient antecedent basis for this limitation in the claim because claim 1 claims "a plurality of processors". Since it had already been established in claim 1 that more than one processor exists,

applicant cannot, is a dependent claim, leave the possibility open that just a single processor can exist.

23. Claim 19 recites the limitation "said breakpoint bit" in lines 4 and 6. There is insufficient antecedent basis for this limitation in the claim because claim 18 claims "at least one breakpoint bit". Therefore, when multiple breakpoint bits exist, it is not clear which of the bits "said breakpoint bit" refers to.

24. Claim 23 recites the limitation "said debug process" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

25. Claim 24 recites the limitation "the attached breakpoint bit" in line 6. There is insufficient antecedent basis for this limitation in the claim because claim 24 previously claims "attaching at least one breakpoint bit". Therefore, when multiple breakpoint bits exist, it is not clear which of the bits "the attached breakpoint bit" refers to.

26. Claim 25 recites the limitation "said breakpoint bit" in lines 2 and 4. There is insufficient antecedent basis for this limitation in the claim because claim 24 claims "at least one breakpoint bit".

27. Claims 3 and 25-29 are rejected under 35 U.S.C 112, 2nd paragraph, for being indefinite, because they are dependent, either directly or indirectly, on an indefinite claim.

Claim Rejections - 35 USC § 102

28. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

29. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Glew et al., U.S. Patent No. 5,694,589 (herein referred to as Glew).

30. Referring to claim 1, Glew has taught an apparatus comprising:

a) a plurality of processors coupled to a controller and a memory. See Fig.1, Fig.3, component 200, and Fig.4. Note that a superscalar processor includes N processing elements to execute up to N instructions in parallel (this is the inherent nature of a superscalar system). Hence, the N processing elements are the plurality of processors, as they each process data.

b) the controller to execute a debug process, said debug process attaches at least one breakpoint bit field to each of a plurality of instructions. See Fig.3, at least component 200, Fig.4, and column 6, lines 24-38.

31. Referring to claim 2, Glew has taught the apparatus of claim 1, wherein said breakpoint bit allows a breakpoint to be one of set and not set for each of said plurality of instructions. See column 6, lines 24-38.

32. Referring to claim 3, Glew has taught the apparatus of claim 2, wherein a breakpoint bit set for an instruction is associated with the address of the instruction. See Fig.3, Fig.4, and column 6, lines 24-38. Note that the address of the instruction is used by the controller to attach the appropriate bit value.

33. Referring to claim 9, Glew has taught the apparatus of claim 1, wherein internal states of each of said plurality of processors are accessible through said debug process. The examiner deems this to be inherent as this is the nature of debugging. During debugging, a user is able to

view the state of the machine (and consequently, of each of the processors) in order to determine how the system is functioning.

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

35. Claims 4-6, 18-22, 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew in view of Deng et al., U.S. Patent No. 6,951,416 (herein referred to as Deng).

36. Referring to claim 4, Glew has taught an apparatus as described in claim 1. Glew has not taught that said controller attaches at least three debug register bit fields to at least one control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field. However, Deng has taught such a concept. See Fig.16 of Deng and note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field. These bits allow for increased functionality and flexibility in debugging. For instance, the enable/disable field allows debugging to be turned on and off, the single-step field allows a break after each instruction, which allows a user to view the effects of each instruction on the system, and the run field allows breakpoints to be enabled/disabled for specific addresses. So, even though an instruction should break because it corresponds to an address, the user may decide skip that break and allow the processor to continue running for whatever reason. As a result, in order to increase flexibility and

functionality, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew such that the controller attaches at least three debug register bit fields to at least one control status register, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field.

37. Referring to claim 5, Glew in view of Deng has taught the apparatus of claim 4, wherein said single step field allows a set of instructions to each be single-stepped through one cycle at a time. See Fig.16, field 206, and column 5, lines 29-33, of Deng.

38. Referring to claim 6, Glew in view of Deng has taught the apparatus of claim 4, wherein said debug enable field one of enables and disables a debug mode. See Fig.16, field 208, of Deng.

39. Referring to claim 18, Glew has taught an apparatus comprising a machine-readable medium containing instructions which, when executed by a machine, cause the machine to perform operations comprising:

a) attaching at least one breakpoint bit field to each of a plurality of instructions. See Fig.3, at least component 200, Fig.4, and column 6, lines 24-38.

b) Glew has not taught attaching at least three debug register bit fields to at least one control status register. However, Deng has taught such a concept. See Fig.16 of Deng and note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field. These bits allow for increased functionality and flexibility in debugging. For instance, the enable/disable field allows debugging to be turned on and off, the single-step field allows a break after each instruction, which allows a user to view the effects of each instruction on the system, and the run field allows breakpoints to be

enabled/disabled for specific addresses. So, even though an instruction should break because it corresponds to an address, the user may decide skip that break and allow the processor to continue running for whatever reason. As a result, in order to increase flexibility and functionality, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew such that at least three debug register bit fields are attached to at least one control status register.

40. Referring to claim 19, Glew in view of Deng has taught the apparatus of claim 18, further containing instructions which, when executed by a machine, cause the machine to perform operations including: determining a state of said breakpoint bit, and setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set. See Glew, column 6, lines 24-38.

41. Referring to claim 20, Glew in view of Deng has taught the apparatus of claim 18, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field. See Fig.16 of Deng and note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field.

42. Referring to claim 21, Glew in view of Deng has taught the apparatus of claim 20, further containing instructions which, when executed by a machine, cause the machine to perform operations including: determining a state of a run field bit, and running a set of instructions if said state of said run field bit is set, and stopping a set of instructions if said state of said run field bit is not set. See Deng, Fig.16, and note that if any first field of four-bit field 202 is enabled, then a set of instructions is stopped when the address associated with the first field. The instructions stopped are the instruction associated with the address and all subsequent

instructions. If the first field is disabled, then the set of instructions will run because the address associated with the first field does not result in a breakpoint.

43. Referring to claim 22, Glew in view of Deng has taught the apparatus of claim 21, further containing instructions which, when executed by a machine, cause the machine to perform operations including: determining a state of a single step bit, single-stepping through a set of instructions for a cycle if said state of said single-step bit is set. See Fig.16, field 206, and column 5, lines 29-33, of Deng.

44. Referring to claim 24, Glew has taught a method comprising:

a) attaching at least one breakpoint bit field to each of a plurality of instructions, wherein the attached breakpoint bit field is an additional field added to each instruction. See Fig.3, at least component 200, Fig.4, and column 6, lines 24-38.

b) Glew has not taught attaching at least three breakpoint register bit fields to at least one control status register. However, Deng has taught such a concept. See Fig.16 of Deng and note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field. These bits allow for increased functionality and flexibility in debugging. For instance, the enable/disable field allows debugging to be turned on and off, the single-step field allows a break after each instruction, which allows a user to view the effects of each instruction on the system, and the run field allows breakpoints to be enabled/disabled for specific addresses. So, even though an instruction should break because it corresponds to an address, the user may decide skip that break and allow the processor to continue running for whatever reason. As a result, in order to increase flexibility and functionality, it would have been obvious to one of ordinary skill in the art at the time of the

invention to modify Glew such that at least three debug register bit fields are attached to at least one control status register.

45. Referring to claim 25, Glew in view of Deng has taught the method of claim 24, further comprising determining a state of said breakpoint bit, and setting a breakpoint for an instruction if it is determined that said state of said breakpoint bit is set. See Glew, column 6, lines 24-38.

46. Referring to claim 26, Glew in view of Deng has taught the method of claim 24, further comprising running a debug process on a host device, and entering debug commands through a graphical user interface. See Deng, column 1, line 50, to column 2, line 9. Note that if a user is stepping through a program, then that user must enter a step command.

47. Referring to claim 27, Glew in view of Deng has taught the method of claim 24, wherein said at least three register bit fields comprise a run field, a single step field and a debug enable field. See Fig.16 of Deng and note field 208, which is a debug enable field, field 206, which is a single-step field, and field 202 (BE1, BE2, BE3, or BE4), which is a run field.

48. Referring to claim 28, Glew in view of Deng has taught the method of claim 24, further comprising: determining a state of a single-step bit, entering commands for single-stepping through a set of instructions for a cycle if said state of said single-step bit is set. See Fig.16, field 206, and column 5, lines 29-33, of Deng.

49. Claims 7-8, 23, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glew.

50. Referring to claim 7, Glew has taught an apparatus as described in claim 1. Glew has not explicitly taught that at least one instruction loads content of at least one register into an

instruction memory coupled to said at least one processor via a bus. However, Official Notice is taken that store instructions and their advantages are well known and accepted in the art. A store instruction, as is known, stores data in a register into an instruction memory (a memory which is accessed by an instruction). Such an instruction allows for increasing the storage space of the program as an amount of data that is too large to store in the register file can also be stored in the memory and retrieved later when necessary. As a result, in order to increase storage flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew to include a store instruction that loads content of at least one register into an instruction memory coupled to said at least one processor via a bus.

51. Referring to claim 8, Glew has taught an apparatus as described in claim 7. Glew has not explicitly taught that content of said instruction memory is loaded into a register coupled to said at least one processor. However, Official Notice is taken that load instructions and their advantages are well known and accepted in the art. A load instruction, as is known, retrieves data from instruction memory (a memory which is accessed by an instruction) and loads the data into a register. Such an instruction allows for increasing the storage space of the program as an amount of data that is too large to store in the register file can also be stored in the memory and retrieved later when necessary. As a result, in order to increase storage flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew to include a load instruction that loads content of said instruction memory into a register coupled to said at least one processor.

52. Referring to claim 23, Glew in view of Deng has taught an apparatus as described in claim 18.

a) Glew has further taught instructions which, when executed by a machine, cause the machine to perform operations including: accessing internal states of each of a plurality of processors through said debug process. The examiner deems this to be inherent as this is the nature of debugging. During debugging, a user is able to view the state of the machine (and consequently, of each of the processors (each superscalar processing element) in order to determine how the system is functioning.

b) Glew in view of Deng has not explicitly taught that the apparatus further contains instructions which, when executed by a machine, cause the machine to perform operations including: loading content of at least one register into an instruction memory and loading content of said instruction memory into the at least one register. However, Official Notice is taken that store and load instructions and their advantages are well known and accepted in the art. A store instruction, as is known, stores data in a register into an instruction memory (a memory which is accessed by an instruction), and a load instruction, as is known, retrieves data from instruction memory (a memory which is accessed by an instruction) and loads the data into a register. Such instructions allow a processor to read and write data to memory, thereby increasing its storage space. As a result, in order to increase storage flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew in view of Deng to include a load content of at least one register into an instruction memory (store instruction) and load content of said instruction memory into the at least one register (load instruction).

53. Referring to claim 29, Glew in view of Deng has taught a method as described in claim 24.

a) Glew has further taught accessing internal states of each of a plurality of processors through said debug process, wherein accessing includes reading state values and overwriting state values. The examiner deems this to be inherent as this is the nature of debugging. During debugging, a user is able to view the state of the machine (and consequently, of each of the processors (each superscalar processing element) and set the state of the machine in order to determine how the system is functioning.

b) Glew in view of Deng has not taught loading content of at least one register into an instruction memory and loading content of said instruction memory into the at least one register. However, Official Notice is taken that store and load instructions and their advantages are well known and accepted in the art. A store instruction, as is known, stores data in a register into an instruction memory (a memory which is accessed by an instruction), and a load instruction, as is known, retrieves data from instruction memory (a memory which is accessed by an instruction) and loads the data into a register. Such instructions allow a processor to read and write data to memory, thereby increasing its storage space. As a result, in order to increase storage flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Glew in view of Deng to include a load content of at least one register into an instruction memory (store instruction) and load content of said instruction memory into the at least one register (load instruction).

Conclusion

54. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the

patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Chen, U.S. Patent Application Publication No. US 2005/0114638 A1, has taught including a halt bit in the instruction opcode for halting execution of that instruction, control register bits for halting execution of individual instructions and multiple instructions.

Deao et al., U.S. Patent No. 6,016,555, has taught a software breakpoint bit which replaces a single opcode bit in order to cause a breakpoint.

Betker et al., U.S. Patent No. 5,889,981, has taught decoding logic which compares instruction addresses to breakpoint addresses and marks a matching instruction so that instead of decoding the instruction, the instruction is transformed into a system breakpoint (sbpt) instruction.

Swoboda et al., U.S. Patent No. 6,567,933, has taught a debug mode which includes, halt and step states, and also allows for the jamming of an instruction into the pipeline so that registers may be read.

IBM Technical Disclosure Bulletin NA8910133 has taught setting a breakpoint bit for each instruction in instruction RAM that should cause a break.

IBM Technical Disclosure Bulletin NA8907370 has taught setting a breakpoint bit for each instruction in instruction RAM that matches a breakpoint address.

Turley, James L., "Advanced 80386 Programming Techniques," Osborne McGraw-Hill, Berkeley, CA, 1988, has taught debugging basics including software and hardware breakpoints and single-stepping.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
June 15, 2007